QSFP28-DR-100G

100GBASE-DR QSFP28 500m Single Mode Fiber Transceiver

Description

The QSFP28-DR-100G, 100GBASE-DR single lambda (wavelength), hot pluggable optical transceiver is a cost focused solution for 100GE links for up to 500m over single mode fiber (SMF). It combines 4x 25 Gb/s NRZ electrical lanes into one 53.125 GBd PAM4 optical channel in compliance with IEEE 100GBASE-DR. Superior performance and reliability is achieved through the advanced transmitter and receiver design using a cooled EA-DFB-LD and a PIN PD with low-power TIA for an average power consumption of 3.5W. The QSFP28-DR-100G supports a RS-FEC (544,514) encoder/decoder function for flexibility with 100GAUI-4 and CAUI-4 interfaces.

Features

- IEEE 100GBASE-DR compliant
- 100GE Single Protocol (103.125 Gb/s)
- CAUI-4 compliant - 4x 25.78125 Gb/s
- 100GAUI-4 compliant – 4x 26.5625 Gb/s
- RS-FEC(544,514) FEC coder/decoder function
- 4.0 W max (3.5 typ.)
- 0 to 70ºC
- Single cooled 100Gb/s 1310nm EML
- Single PIN PD + low-power TIA
- SFF-8636 management interface

Applications

- Data Center 100GE 500m SMF links
- 4:1 breakout with 400GBASE-DR4
- Switch/Router interconnections

CONTENTS

1 FUNCTIONAL DESCRIPTION

The QSFP28-DR-100G is a fully integrated, 103.125 Gb/s single optical channel transceiver. The optical channel uses a 4-level pulse amplitude modulation (PAM4) format by means of a DSP, a 1310 nm wavelength EA-DFB laser diode, a PIN photo-diode connecting to a NRZ-based 4 channel x 25.78125 Gb/s CAUI-4 or 4-channel x 26.5625 Gb/s 100GAUI-4 electrical interface by means of a 4:1 mux/demux. This single optical channel technology enables a cost-optimized solution for 100GE optical links. The embedded RS-FEC (544,514) function provides flexibility for compatibility between hosts with CAUI-4 or 100GAUI-4 electrical interfaces. The SFF-8636 compliant 2-wire management interface enables control, alarm and monitoring of the QSFP28 module,

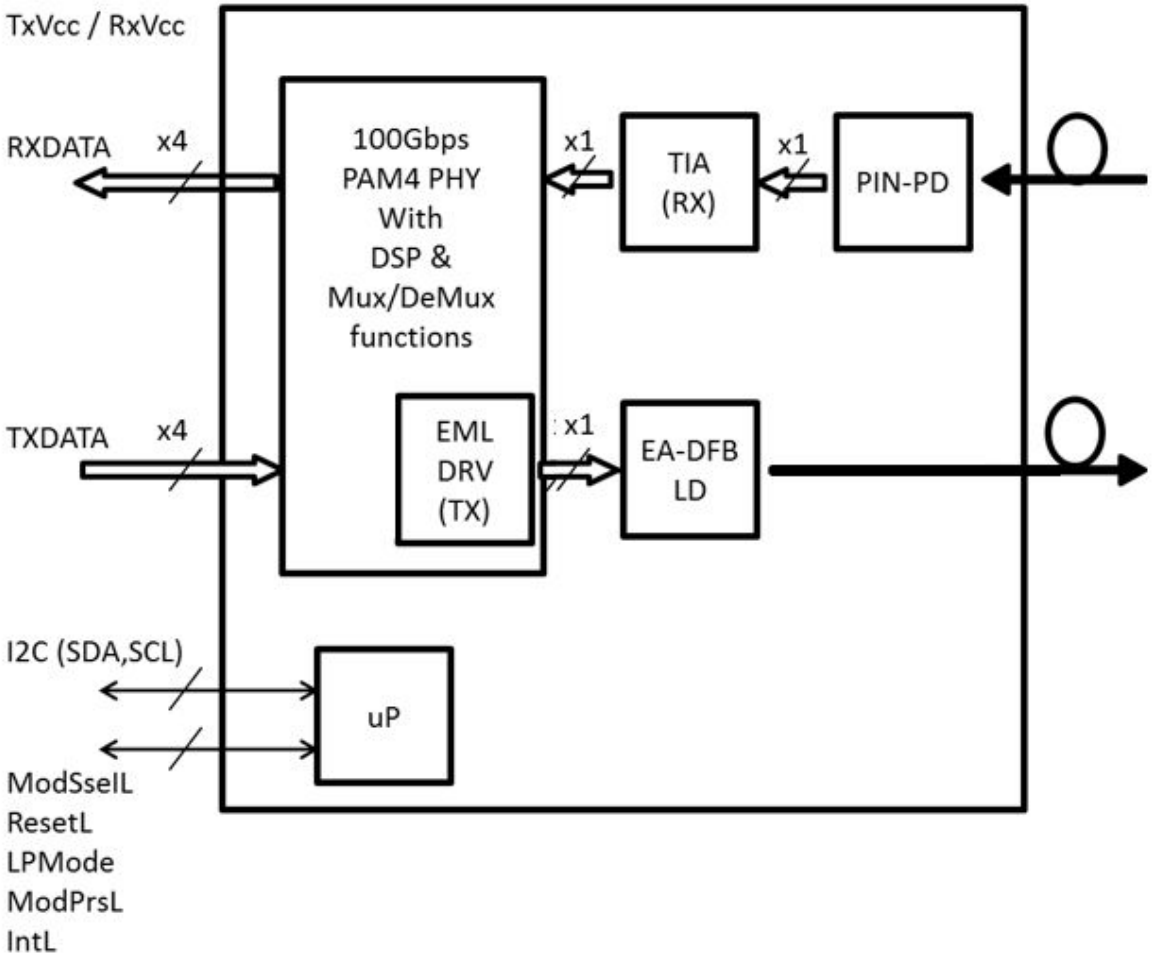

Figure 1 Functional Block Diagram

2 PERFORMANCE SPECIFICATIONS

2.1 Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings will cause permanent damage and/or adversely affect device reliability.

Table 1 Absolute Maximum Ratings

No.	Parameter	Symbol	Min.	Max.	Unit	Remarks
1	Supply Voltage	Vcc	0	+3.6	V	+3.3 V
2	Storage Temperature		-40	85	°C	
3	Optical Receiver Input		-	+5.0	dBm	Average

2.2 Operating Environments

Electrical and optical characteristics below are defined under this operating environment, unless otherwise specified.

Table 2 Operating Environment

No	Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
1	Supply Voltage	Vcc	3.135	3.3	3.465	V	
2	Supply Voltage Noise Tolerance	PSNR	-	-	66	mV	10 Hz –10 MHz
3	Power Consumption		-	-	4.0	W	
4	Supply Current		--	-	1275.97	mA	Steady state
5	Case Temperature	TC	0	25	70	°C	

2.3 Electrical Interface

Table 3 Electrical Characteristics

No.	Parameter	Min.	Typ.	Max.	Unit	Remarks
Transmitter (each lane)						
1	Differential pk-pk input voltage tolerance (min)	900	-	-	mV	at TP1a
2	Differential termination mismatch	-	-	10	%	at TP1
3	Single-ended input voltage tolerance range	-0.4 to 3.3	-	-	V	at TP1a
4	DC common mode voltage	-350	-	2850	mV	at TP1
Receiver (each lane, at TP4)						
1	AC Common-mode output voltage (RMS)	-	-	17.5	mV	
2	Differential output voltage	-	-	900	mV	
3	Eye width	0.57	-	-	UI	
4	Eye height, differential	228	-	-	mV	
5	Vertical eye closure	-	-	5.5	dB	
6	Differential termination mismatch	-	-	10	%	
7	Transition time (20% to 80%)	12	-	-	ps	
8	DC common mode voltage	-350	-	2850	mV	

Note 1: Electrical Rx output is squelched for loss of optical input signal.

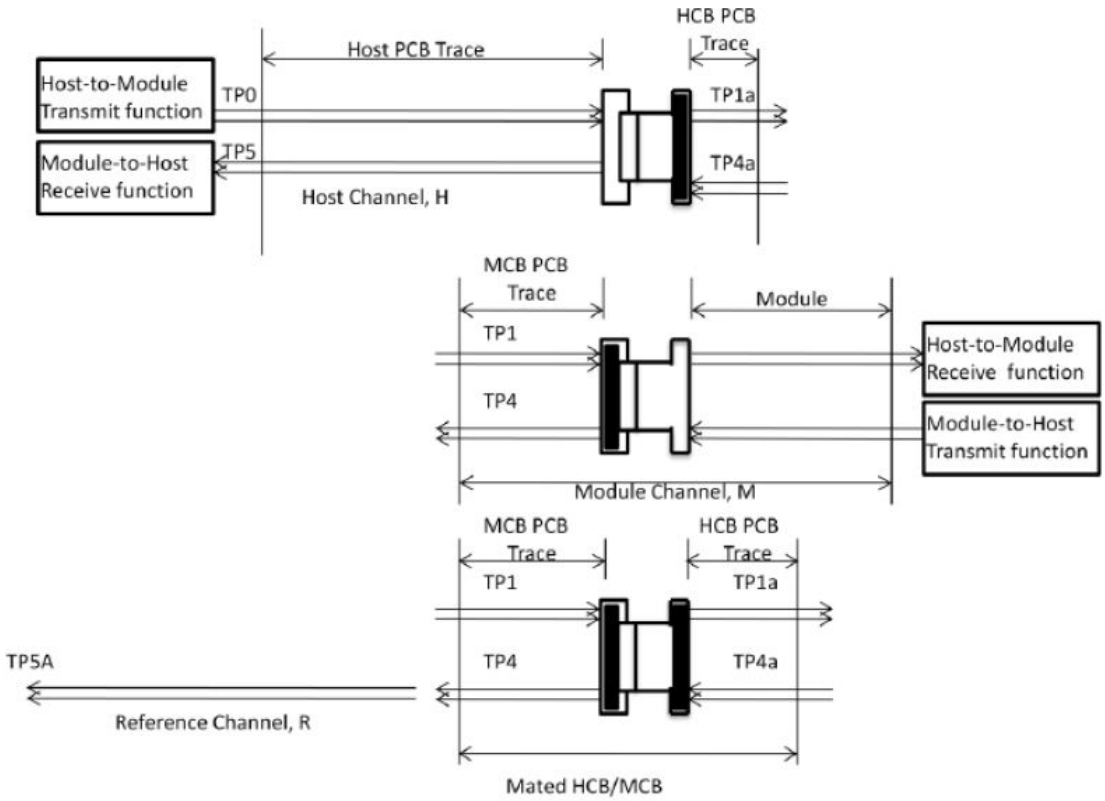

Figure 2 Reference Test Points

2.4 Optical Interface

Table 4 Transmitter Characteristics

No.	Description	Value	Unit
1	PAM4 Signaling rate (range)	53.125 ± 100 ppm	GBd
2	Lane wavelengths (range)	1304.5- 1317.5	nm
3	Side-mode suppression ratio (SMSR), (min)	30	dB
4	Average launch power, (max)	4	dBm
5	Average launch power[1] (min)	-2.9	dBm
6	Outer Optical Modulation Amplitude (OMAouter) (max)	4.2	dBm
7	Outer Optical Modulation Amplitude (OMAouter)[2] (min)	-0.8	dBm
8	Launch power in OMAouter minus TDECQ (min) ER≥5dB[2]	-2.2	dBm
9	Launch power in OMAouter minus TDECQ (min) ER<5dB[2]	-1.9	dBm
10	Transmitter and dispersion penalty Eye Closure for PAM4 (TDECQ), (max)	3.4	dB
11	TDECQ – $10*\log_{10}(C_{eq})$ (max)[4]	3.4	dB
12	Average launch power of OFF transmitter (max)	-15	dBm
13	Extinction ratio (min)	3.5	dB
14	Optical return loss tolerance (max)	15.5	dB
15	Transmitter reflectance[3] (max)	-26	dB
16	Transmitter transition time (max)	17	ps
17	$RIN_{15.5}$ OMA (max)	-136	dB/Hz

Note 1: Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.

Note 2: Even if the TDECQ < 1.4 dB for an extinction ratio of ≥ 5 dB or TDECQ < 1.1dB for an extinction ratio of < 5 dB, the OMAouter (min) must exceed this value.

Note 3: Transmitter reflectance is defined looking into the transmitter.

Note 4: Ceq is a coefficient defined in IEEE Std 802.3-2018 clause 121.8.5.3 which accounts for reference equalizer noise enhancement.

Table 5 Receiver Characteristics

No.	Description	Value	Unit
1	PAM4 Signaling rate (range)	53.125 ± 100 ppm	GBd
2	Lane wavelengths (range)	1304.5 to 1317.5	Nm
3	Damage threshold[1] (min)	5	dBm
4	Average receive power (max)	4	dBm
5	Average receive power[2] (min)	-5.9	dBm
6	Receive power (OMAouter) (max)	4.2	dBm
7	Receiver reflectance (max)	-26	dB
8	Receiver sensitivity (OMAouter)[3] (max)	−3.9, $SECQ$−5.3, (See Figure 3)	dBm
9	Stressed receiver sensitivity (OMAouter)[4] (max)	-1.9	
Conditions of stressed receiver sensitivity test[5]:			
10	Stressed eye closure for PAM4 (SECQ)	3.4	dB
11	SECQ – 10*$\log_{10}$(Ceq) (max)[6]	3.4	dB

Note 1: The receiver shall be able to tolerate, without damage, continuous exposure to an optical signal having this average power level

Note 2: Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.

Note 3: Receiver sensitivity (OMAouter), (max) is informative and is defined for a transmitter with a value of SECQ up to 3.4 dB.

Note 4: Measured with conformance test signal at TP3 (see IEEE Std 802.3cd clause 140.7.10) for the BER specified in IEEE Std 802.3cd clause 140.1.1.

Note 5: These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Note 6: Ceq is a coefficient defined in IEEE Std 802.3-2018 clause 121.8.5.3 which accounts for reference equalizer noise enhancement.

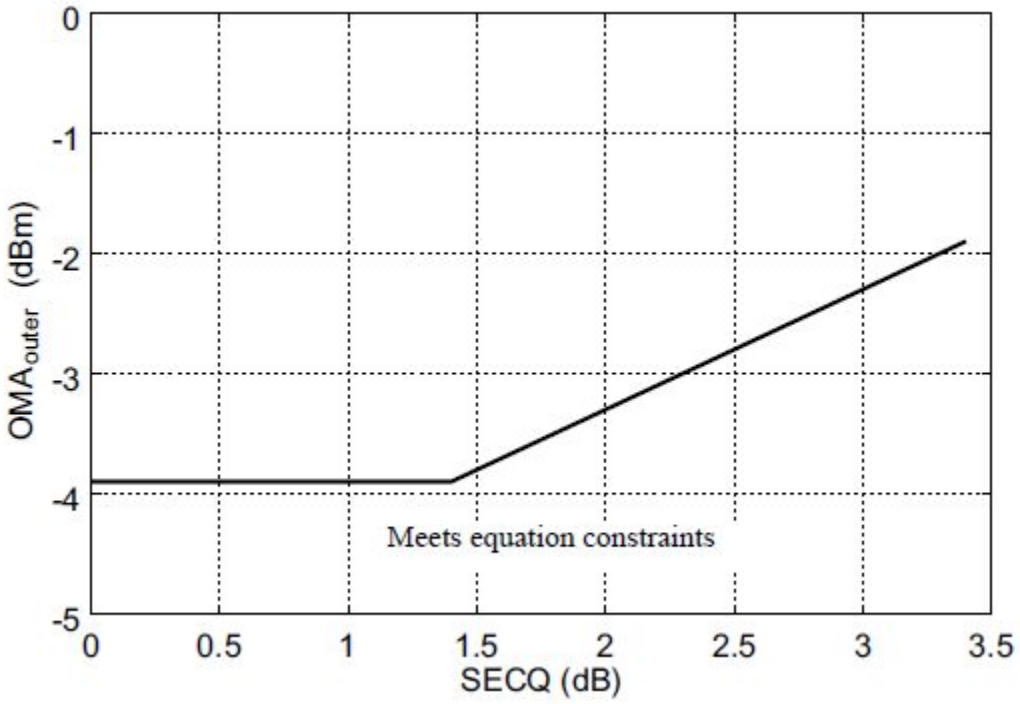

Figure 3 Receiver Sensitivity

Table 6 RX_LOS Alarm Characteristics

No.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
1	Receiver Loss of Signal Indicator Assert Level	RX_LOS	-30	-	-7.5	dBm	Average power
2	Receiver Loss of Signal Indicator De-assert Level	RX_LOS	-	-	-7	dBm	Average power

3 HIGH SPEED DATA INTERFACE

3.1 Rx(n)(p/n)

Rx(n)(p/n) are module receiver data outputs. Rx(n)(p/n) are AC-coupled 100 Ohm differential lines that should be terminated with 100 Ohm differentially at the Host ASIC (SerDes). The AC coupling is inside the module and not required on the Host board.

Output squelch for loss of optical input signal, hereafter Rx Squelch shall function as follows. In the event of the optical signal on any channel becoming equal to or less than the level required to assert LOS, then the receiver data output for that channel shall be squelched or disabled. In the squelched or disabled state output impedance levels are maintained while the differential voltage swing shall be less than 50 mVpp.

3.2 Tx(n)(p/n)

Tx(n)(p/n) are module transmitter data inputs. They are AC-coupled 100 Ohm differential lines with 100 Ohm differential terminations inside the module. The AC coupling is inside the module and not required on the Host board.

Output squelch, hereafter Tx Squelch, for loss of input signal, hereafter Tx LOS, is supported. In the event of the differential, peak-to-peak electrical signal on any channel becomes less than 50 mVpp, then the transmitter optical output for that channel shall be squelched and the associated TxLOS flag set. Where squelched, the transmitter OMA shall be less than or equal to -26 dBm.

4 CONTROL INTERFACE

4.1 Low Speed Control Pins

In addition to the 2-wire serial interface the transceiver has the following low speed pins for control and status: ModSelL, ResetL, LPMode, ModPrsL and IntL.

4.1.1 ModSelL

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple modules on a single 2-wire interface bus. When the ModSelL, is “High”, the module shall not respond to or acknowledge any 2-wire interface communication from the host. ModSelL signal input node shall be biased to the “High” state in the module. In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the ModSelL de-assert time after any modules are deselected. Similarly, the host shall wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met.

4.1.2 ResetL

The ResetL pin shall be pulled to Vcc in the module. A low level on the ResetL pin for longer than the minimum pulse length initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by asserting “low" an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

4.1.3 LPMode

The LPMode pin shall be pulled up to Vcc in the module. The pin is a hardware control used to put modules into a low power mode when high. By using the LPMode pin and a combination of the Power_override, Power_set and High_Power_Class_Enable software control bits (Address A0h, byte 93 bits 0,1,2), the host controls how much power a module can dissipate.

4.1.4 ModPrsL

ModPrsL is pulled up to Vcc_Host on the host board and grounded in the module. The ModPrsL is asserted “Low" when inserted and de-asserted “High” when the module is physically absent from the host

connector.

4.1.5 IntL

IntL is an output pin. When IntL is “Low,” it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and shall be pulled to host supply voltage on the host board. The IntL pin is de-asserted “High” after completion of reset, when byte 2 bit 0 (Data Not Ready) is read with a value of “0” and the flag field is read (see SFF-8636).

4.2 2-Wire Management Interface

A management interface is specified in order to enable flexible use of the module by the user. The QSFP28 Module supports alarm, control and monitor functions via a two-wire interface bus. Upon module initialization, these functions are available. QSFP28 two-wire electrical interface consists of 2 pins of SCL (2-wire serial interface clock) and SDA (2-wire serial interface data). The timing requirements on the two-wire interface are listed in Table 8 and Fig. 4.

Table 7 Low Speed Control and Sense Signals

Parameter	Symbol	Min	Max	Unit	Condition
SCL and SDA	VOL	0	0.4	V	IOL(max)=3.0mA
	VOH	Vcc-0.5	Vcc+0.3	V	
SCL and SDA	VIL	-0.3	Vcc*0.3	V	
	VIH	VCC*0.7	Vcc + 0.5	V	
Capacitance for SCL and SDA I/O pin	Ci		14	pF	
Total bus capacitive load for SCL and SDA	Cb		100	pF	3.0 k Ohms pull-up resistor, max
			200	pF	1.6 k Ohms pull-up resistor max
LPMode, Reset and ModSelL	VIL	-0.3	0.8	V	
	VIH	2	VCC+0.3	V	
	Iin	-365	125	uA	0 V ≤ Vin ≤ Vcc
ModPrsL and IntL	VOL	0	0.4	V	IOL=2.0mA
	VOH	VCC-0.5	VCC+0.3	V	

Table 8 2-Wire Management Interface Timing Parameters

Parameter	Symbol	Min	Max	Unit	Conditions
Clock Frequency	f_{SCL}	0	400	kHz	
Clock Pulse Width Low	t_{LOW}	1.3	-	μs	
Clock Pulse Width High	t_{HIGH}	0.6	-	μs	
Time bus free before new transaction can start	t_{BUF}	20	-	μs	Between STOP and START and between ACK and Restart
START Hold time	$t_{HD,STA}$	0.6	-	μs	
START Set-Up time	$t_{SU,STA}$	0.6	-	μs	
Data in Hold time	$t_{HD,DAT}$	0	-	μs	
Data in Set-Up time	$t_{SU,DAT}$	0.1	-	μs	
Input Rise time (400 kHz)	$t_{R,400}$	-	300	ns	Note 1
Input Fall time (400 kHz)	$t_{F,400}$	-	300	ns	Note 2
STOP Set-Up time	$t_{SU,STO}$	0.6	-	μs	
Serial Interface Clock Holdoff “Clock Stretching”	T_clock_hold	-	500	μs	Maximum time the slave (QSFP28) may hold the SCL line low before continuing read or write operation
Complete Single or Sequential Write	t_{WR}	-	40	ms	Complete (up to) 4 Byte Write
Endurance (Write Cycles)		50k		Cycles	60°C

Note 1: From (VIL,MAX – 0.15) to (VIH,MIN + 0.15)

Note 2: From (VIH,MIN + 0.15) to (VIL,MAX - 0.15)

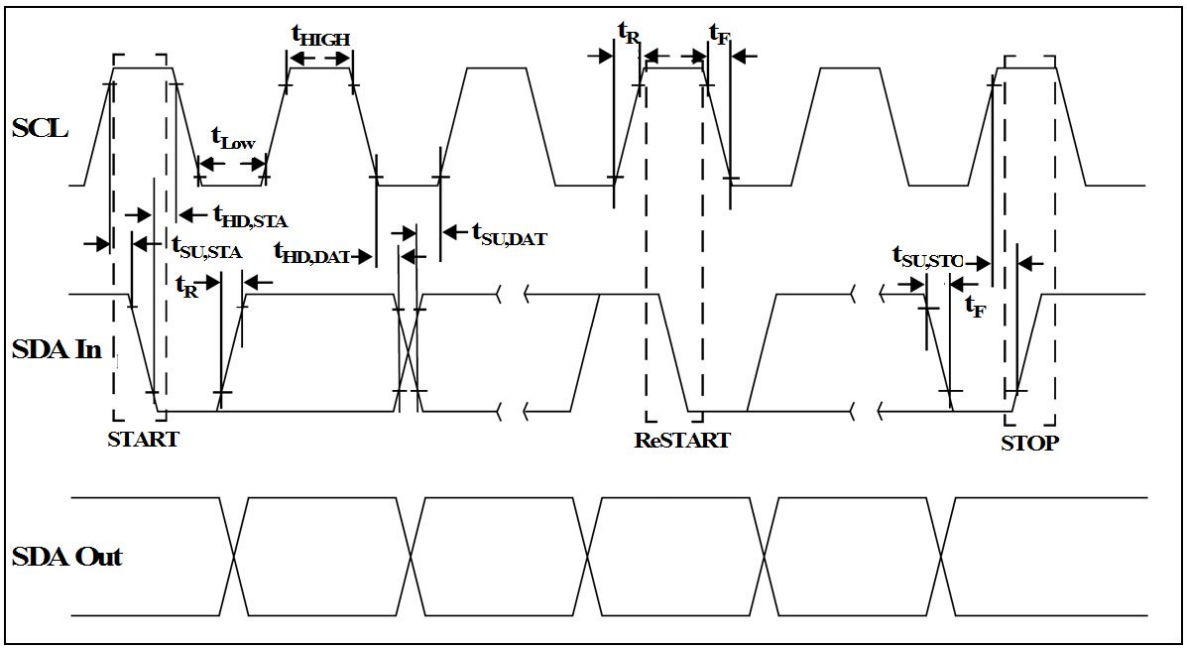

Figure 4 2-Wire Interface Timing Diagram

4.3 Soft Control and Status Functions

Table 9 lists the required timing performance for software controlled control and status functions.

Table 9 Control and Status Timing Requirements

Parameter	Symbol	Min	Max	Unit	Conditions	Notes
Initialization time	t_init		10	s	Time from power on or hot plug until the module is fully functional. This time applies to Power Class 2 or higher modules when LPMode is pulled low by the host, and to all Power Class 1 modules.	2,3,6
Reset Init Assert Time	t_reset_init	10	-	μs	Host is required to provide a reset pulse of at least the minimum value for the module to guarantee a reset sequence. Shorter pulses may reset the module depending on implementation.	
Serial Bus Hardware Ready Time	t_serial		2	s	Time from power on until the module responds to data transmission over the two-wire serial bus.	2
Monitor Data Ready Time	t_data		2	s	Time from power on to Data_Not_Ready, Byte 2 bit 0, cleared to 0 and IntL output pulled low.	2
Reset Assert Time	t_reset		10	s	Time from a rising edge on the ResetL input until the module is fully functional.	3
LPMode/TxDis mode change time	t_LPMode/TxDis		100	ms	Time to change between LPMode and TxDis modes of the dual- mode signal LPMode/TxDis	

Parameter	Symbol	Min	Max	Unit	Conditions	Notes
LPMode Assert Time	ton_LPMode		100	ms	Time from when the host releases LPMode to high until module power consumption reaches Power Class 1.	
LPMode Deassert Time	toff_LPMode		1500	ms	Time from when the host pulls LPMode low until the module is fully functional.	3, 5
IntL/RxLOSL mode change time	t_IntL/RxLOSL		100	ms	Time to change between IntL and RxLOSL modes of the dual - mode signal IntL/RxLOSL.	
IntL Assert Time	ton_IntL		200	ms	Time from occurrence of condition triggering an interrupt until IntL is low.	
IntL Deassert Time	toff_IntL		500	μs	Time from clear on read operation of associated flag until module releases IntL to high. This includes the time to clear Rx LOS, Tx Fault and other flag bits.	4
RxLOSL Assert Time (Optional Fast Mode)	ton_f_LOS		1	ms	Optional fast mode is advertised via the management interface (SFF-8636). Time from optical loss of signal to RxLOSL signal pulled low by the module.	
RxLOSL Deassert Time (Optional Fast Mode)	toff_f_LOS		3	ms	Optional fast mode is advertised via the management interface (SFF-8636). Time from optical signal above the LOS deassert threshold to when the module releases the RxLOSL signal to high.	
Rx LOS Assert Time	ton_LOS		100	ms	Time from Rx optical signal loss to Rx LOS bit set to 1 and IntL pulled low by the module.	
Tx Fault Assert Time	ton_Txfault		200	ms	Time from Tx Fault state to Tx Fault bit set to 1 and IntL pulled low by the module.	

Parameter	Symbol	Min	Max	Unit	Conditions	Notes
Flag Assert Time	ton_flag		200	ms	Time from condition triggering flag to associated flag bit set to 1 and IntL pulled low by the module.	
Mask Assert Time	ton_mask		100	ms	Time from mask bit set to 1 until the module is prevented from pulling IntL low when the associated flag is set high.	1
Mask De-assert Time	toff_mask		100	ms	Time from mask bit cleared to 0 until module is enabled to pull IntL low when the associated flag is set high.	1
Application or Rate Select Change Time	t_ratesel		N/A (Rate Select function not supported)	ms	Time from change of Application Select Byte or Rate Select bit until module is in conformance with the appropriate specifications for the new application or rate	1, 7
Power_override or Power_set Assert Time	ton_Pdown		100	ms	Time from Power_override or Power_Set bit set to 1 until module power consumption reaches Power Class 1.	1
Power_override or Power_set De-assert Time	toff_Pdown		10	s	Time from Power_override or Power_Set bit cleared to 0 until the module is fully functional.	1

Note 1: Measured from rising edge of SDA during STOP sequence of write transaction.

Note 2: Power on is defined as the instant when supply voltages reach and remain at or above the minimum level specified in Table 10.

Note 3: Fully functional is defined as the module being ready to transmit and receive valid signals and all management interface data, including monitors, being valid. It is indicated after Reset or hot plug by the module releasing IntL to high after the host has read a 0 from the Data_Not_Ready flag bit.

Note 4: Measured from rising edge of SDA during STOP sequence of read transaction.

Note 5: Does not apply to Power Class 1 modules.

Note 6: For some modules this limit is overridden via the management interface, SFF -8636, or by custom product specifications.

Note 7: For Fibre Channel speed negotiation, the 100 ms limit is too slow. See the relevant standard for details of the timing requirements.

4.4 FEC Control Function

The QSFP28 Module supports RS(544,514) FEC coder/decoder function as per IEEE Std 802.3-2018, Section 6, Clause 91 [2] on the network side. This FEC coder/decoder function can be bypassed by the host via register page 03h byte 230 of EEPROM register map. When the host supports CAUI-4 interface, the host shall disable KR4 FEC of the host ASIC and the FEC coder/decoder function of the QSFP28 shall be activated. When the host supports 100GAUI-4 interface, the host shall set the FEC coder/decoder function of the QSFP28 bypassed.

4.5 Squelch and TxRx Disable Assert, De-assert and Enable/Disable Timing

Table 10 lists the required timing performance for assert, de-assert, enable and disable of the Tx Squelch, Rx Squelch, Tx Disable and Rx Output Disable functions.

Table 10 Squelch & TxRx Disable Timing

Parameter	Symbol	Max	Unit	Conditions	Note
Rx Squelch Assert Time	ton_Rxsq	15	ms	Time from loss of Rx input signal until the squelched output condition is reached	
Rx Squelch De-assert Time	toff_Rxsq	1500	ms	Time from resumption of Rx input signals until normal Rx output condition is reached.	
Tx Squelch Assert Time	ton_Txsq	400	ms	Time from loss of Tx input signal until the squelched output condition is reached.	
Tx Squelch De-assert Time	toff_Txsq	1500	ms	Time from resumption of Tx input signals until normal Tx output condition is reached.	
Tx Disable Assert Time	ton_TxDis	100	ms	Time from Tx Disable bit set to 1 until optical output falls below 10% of nominal.	1
Tx Disable De-assert Time	toff_TxDis	400	ms	Time from Tx Disable bit cleared to 0 until optical output rises above 90% of nominal.	1
Tx Disable Assert Time (Optional Fast Mode)	ton_f_TxDis	3	ms	Optional fast mode is advertised via the management interface (SFF-8636). Time from TxDis signal high to the optical output reaching the disabled level.	
Tx Disable De-assert Time (Optional Fast Mode)	Toff_f_TxDis	10	ms	Optional fast mode is advertised via the management interface (SFF- 8636). Time from TxDis signal low to the optical output reaching the enabled level.	
Rx Output	ton_RxDis	100	ms	Time from Rx Output Disable bit set to 1 until Rx	1

Parameter	Symbol	Max	Unit	Conditions	Note
Disable Assert Time				output falls below 10% of nominal.	
Rx Output Disable De-assert Time	toff_RxDis	100	ms	Time from Rx Output Disable bit cleared to 0 until Rx output rises above 90% of nominal.	1
Squelch Disable Assert Time	ton_sqDIS	100	ms	This applies to Rx and Tx Squelch and is the time from bit cleared to 0 until squelch functionality is disabled.	1
Squelch Disable De-assert Time	toff_RxDis	100	ms	This applies to Rx and Tx Squelch and is the time from bit set to 1 until squelch functionality is enabled.	1

Note 1: Measured from rising edge of SDA during STOP sequence of write transaction.

5 POWER

QSFP28 modules are categorized into several power classes as listed in Table 11. The power class of QSFP28-DR-100G is class 5.

Table 11 Maximum Power Classes

Power Class	Maximum power dissipation per module (W)
1	1.5
2	2.0
3	2.5
4	3.5
5	4.0
6	4.5
7	5.0

5.1 Host Board Power Supply Filtering

The host board should use the power supply filtering equivalent to that shown in Figure 3.

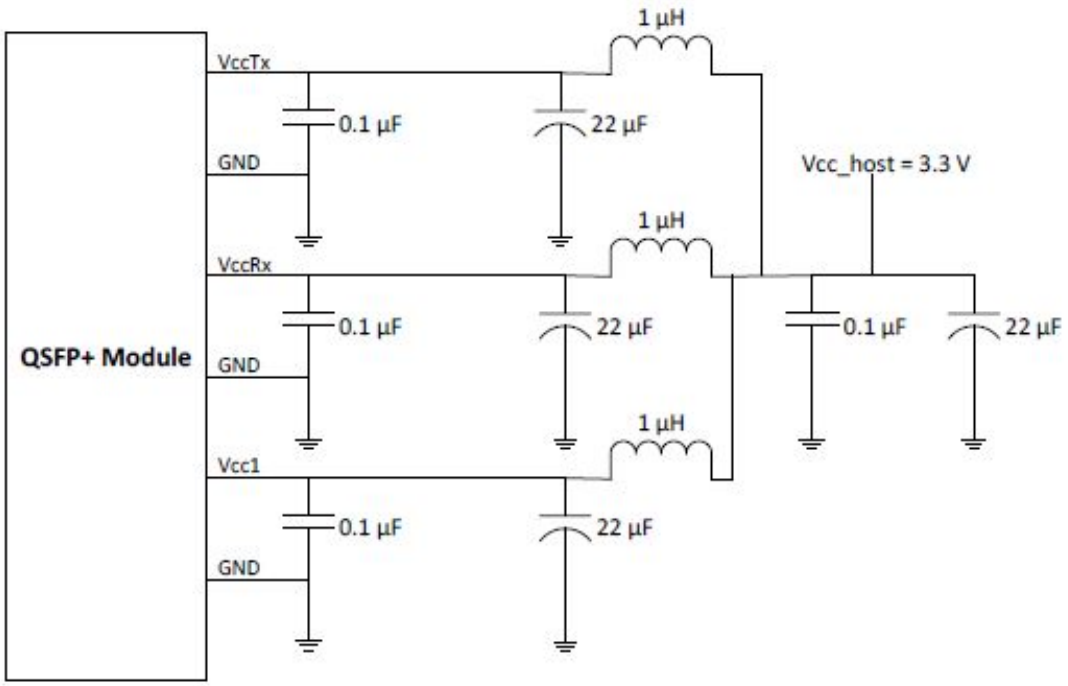

Figure 5 Recommended Host Board Power Supply Filtering

5.2 Power Supply Pins

The circuit card in a QSFP28 module has three designated power pins, labeled VccTx, VccRx and Vcc1. When the QSFP28 module is “hot plugged” into a connector with power already present, the three pins have power applied concurrently. The module is responsible for limiting the inrush current surge during a hot plug event. The host power supply is responsible for supplying up to the maximum inrush current limits during a hot plug event without causing disturbance to other modules and components on the same power supply.

5.3 Module Power Supply Specification

SFF-8679 defines all QSFP28 modules shall power up in power class 1, designated as “Low Power Mode” in order to avoid exceeding the host system power capacity, upon hot-plug, power cycle or reset. QSFP28-DR-100G will reach fully functional operation regardless of whether the host system enables “High Power Mode” which is defined as the maximum power class as advertised in page 00, byte 129. The host system controls using the LPMode input pin and by writing to 3 control bits in byte 93. The management interface specification, SFF-8636 provides complete details but for explanation of power supply control.

6 PIN ASSIGNMENT

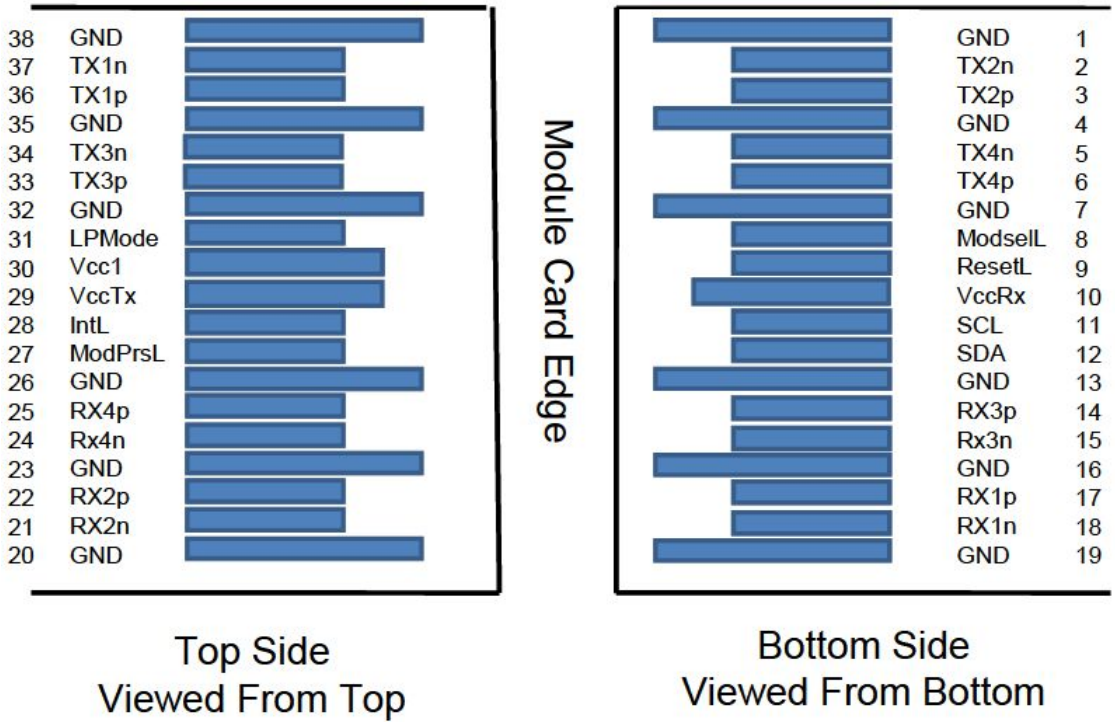

Figure 6 Module Pads