100G QSFP28 CWDM4 Transceivers

PRODUCT FEATURES

- 4 CWDM lanes Mux/De-mux design
- Build in CDR on both TX and RX
- Up to 25.78Gbps Data rate per wavelength
- Up to 2km transmission on SMF
- Electrically hot-pluggable
- Digital Diagnostics Monitoring Interface
- Compliant with QSFP28 MSA with LC connector
- Case operating temperature range:0°C to 70°C
- Power dissipation < 3.5 W

APPLICATIONS

- 100G Ethernet

STANDARD

- Compliant to IEEE 802.3ba and 100G CLR4/CWDM4
- Compliant to SFF-8636
- RoHS Compliant.

General Description

100G QSFP28 CWDM4 is designed to operate over single-mode fiber system using 4X25 CWDM channel in 1310 band and links up to 2km. The module converts 4 inputs channel of 25Gb/s electrical data to 4 CWDM optical signals, and multiplexes them into a single channel for 100Gb/s optical transmission. Reversely, on the receiver side, the module optically de-multiplexes a 100Gb/s input into 4 CWDM channels signals, and converts them to 4 channel output electrical data.

The central wavelengths of the 4 CWDM channels are 1271, 1291, 1311 and 1331 nm. It contains a duplex LC connector for the optical interface and a 38-pin connector for the electrical interface. Single-mode fiber (SMF) is applied in this module. This product converts the 4-channel 25Gb/s electrical input data into CWDM optical signals (light), by a 4-wavelength Distributed Feedback Laser (DFB) TO. The 4 wavelengths are multiplexed into a single 100Gb/s data, propagating out of the transmitter module via the SMF. The receiver module accepts the 100Gb/s optical signals input, and de-multiplexes it into 4 CWDM 25Gb/s channels. Each wavelength light is collected by a discrete photo diode, and then outputted as electric data after amplified by a TIA.

The product is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP28 Multi-Source Agreement (MSA) and compliant to IEEE 802.3ba.

Ⅰ Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Storage Temperature	Ts	-40	-	85	℃	
Relative Humidity	RH	5	-	95	%	
Power Supply Voltage	VCC	-0.3	-	4	V	
Signal Input Voltage		Vcc-0.3	-	Vcc+0.3	V	

Ⅱ Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Case Operating Temperature	Tcase	0	-	70	℃	Without air flow
Power Supply Voltage	VCC	3.13	3.3	3.47	V	
Power Supply Current	ICC	-		1060	mA	
Data Rate	BR		25.78125		Gbps	Each channel
Transmission Distance	TD		-	2	km	
Coupled fiber	Single mode fiber					9/125um SMF

Ⅲ Optical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	NOTE
Transmitter						
Wavelength Assignment	λ 0	1264.5	1271	1277.5	nm	
	λ 1	1284.5	1291	1297.5	nm	
	λ 2	1304.5	1311	1317.5	nm	
	λ 3	1324.5	1331	1337.5	nm	
Total Output. Power	POUT			8.5	dBm	
Average Launch Power Per lane		-6.5		2.5	dBm	
Spectral Width (-20dB)	σ			1	nm	
SMSR		30			dB	
Optical Extinction Ratio	ER	3.5			dB	
Average launch Power off per lane	Poff			-30	dBm	
Transmitter and Dispersion Penalty per lane	TDP			3	dB	
RIN	RIN			-130	dB/Hz	
Output Eye Mask definition {X1，X2，X3，Y1，Y2，Y3}	{0.31，0.4，0.45，0.34，0.38，0.4}					1
Receiver						
Rx Sensitivity per lane	RSENS			-11.5	dBm	2
Input Saturation Power (Overload)	Psat			2.5	dBm	
Receiver Reflectance	Rr			-26	dB	

Notes:

1. Hit ratio $5x10^{-5}$.
2. Measured with a PRBS 2^{31}-1 test pattern, @25.78Gb/s, BER< $5x10^{-5}$.

IV. Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	NOTE
Supply Voltage	Vcc	3.13	3.3	3.47	V	
Supply Current	Icc			1060	mA	
Transmitter						
Input differential impedance	Rin		100		Ω	1
Differential data input swing	Vin,pp	180		1000	mV	
Transmit Disable Voltage	VD	Vcc–1.3		Vcc	V	
Transmit Enable Voltage	VEN	Vee		Vee+ 0.8	V	2
Receiver						

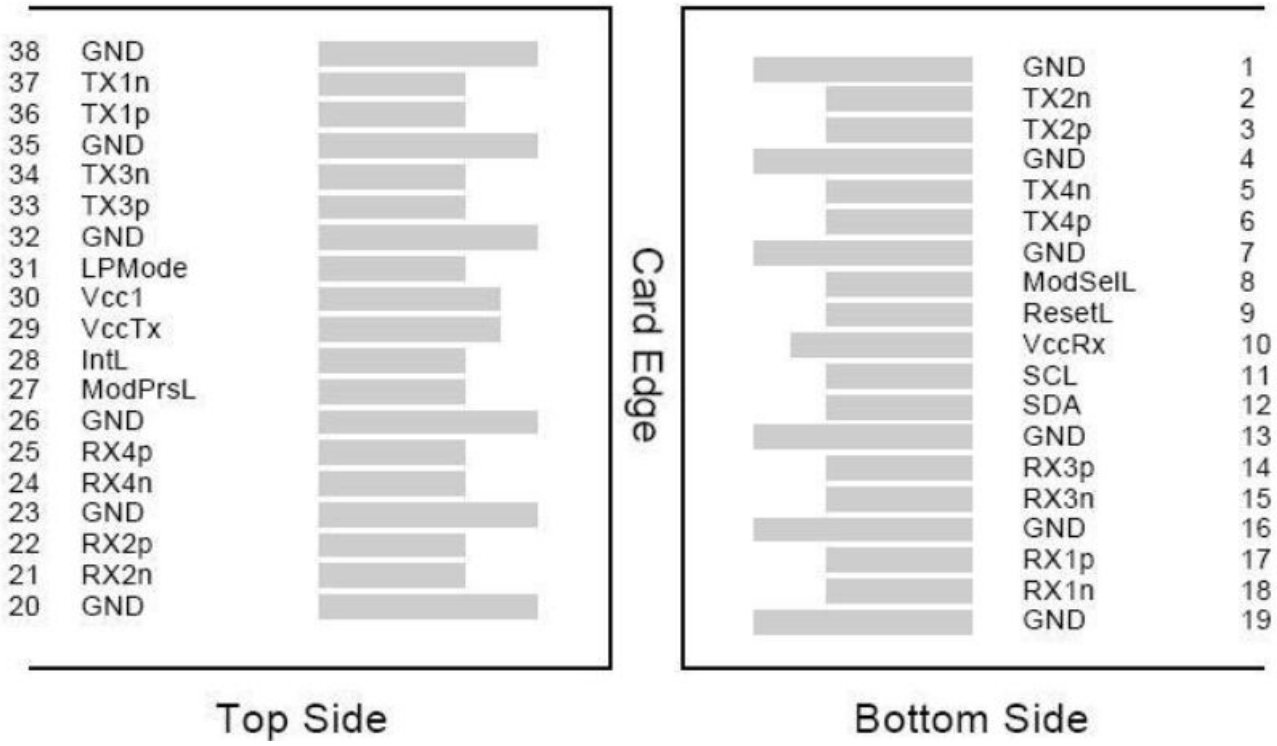
Differential data output swing	Vout,pp	300		850	mV	3

Notes:

1. Connected directly to TX data input pins. AC coupled thereafter.
2. Or open circuit.
3. Into 100 ohms differential termination.

V. Pin Assignment

Figure 1---Pin out of Connector Block on Host Board



Pin	Symbol	Name/Description	NOTE
1	GND	Transmitter Ground (Common with Receiver Ground)	1
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data output	
4	GND	Transmitter Ground (Common with Receiver Ground)	1
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data output	
7	GND	Transmitter Ground (Common with Receiver Ground)	1
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	VccRx	3.3V Power Supply Receiver	2
11	SCL	2-Wire serial Interface Clock	
12	SDA	2-Wire serial Interface Data	
13	GND	Transmitter Ground (Common with Receiver Ground)	
14	Rx3p	Receiver Non-Inverted Data Output	
15	Rx3n	Receiver Inverted Data Output	
16	GND	Transmitter Ground (Common with Receiver Ground)	1
17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1n	Receiver Inverted Data Output	

19	GND	Transmitter Ground (Common with Receiver Ground)	1
20	GND	Transmitter Ground (Common with Receiver Ground)	1
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver Non-Inverted Data Output	
23	GND	Transmitter Ground (Common with Receiver Ground)	1
24	Rx4n	Receiver Inverted Data Output	1
25	Rx4p	Receiver Non-Inverted Data Output	
26	GND	Transmitter Ground (Common with Receiver Ground)	1
27	ModPrsl	Module Present	
28	IntL	Interrupt	
29	VccTx	3.3V power supply transmitter	2
30	Vcc1	3.3V power supply	2
31	LPMode	Low Power Mode	
32	GND	Transmitter Ground (Common with Receiver Ground)	1
33	Tx3p	Transmitter Non-Inverted Data Input	
34	Tx3n	Transmitter Inverted Data Output	
35	GND	Transmitter Ground (Common with Receiver Ground)	1
36	Tx1p	Transmitter Non-Inverted Data Input	
37	Tx1n	Transmitter Inverted Data Output	
38	GND	Transmitter Ground (Common with Receiver Ground)	1

Notes:

1. GND is the symbol for signal and supply (power) common for QSFP28 modules. All are common within the QSFP28 module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.

2. VccRx, Vcc1 and VccTx are the receiving and transmission power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown below. Vcc Rx, Vcc1 and Vcc Tx may be internally connected within the QSFP28 transceiver module in any combination. The connector pins are each rated for a maximum current of 500mA.

VI. Digital Diagnostic Functions

The QSFP28 CWDM4 transceivers support the 2-wire serial communication protocol as defined in the QSFP28 MSA. Which allows real-time access to the following operating parameters:

- Transceiver temperature
- Laser bias current
- Transmitted optical power
- Received optical power
- Transceiver supply voltage

It also provides a sophisticated system of alarm and warning flags, which may be used to alert end-users when particular operating parameters are outside of a factory-set normal range.

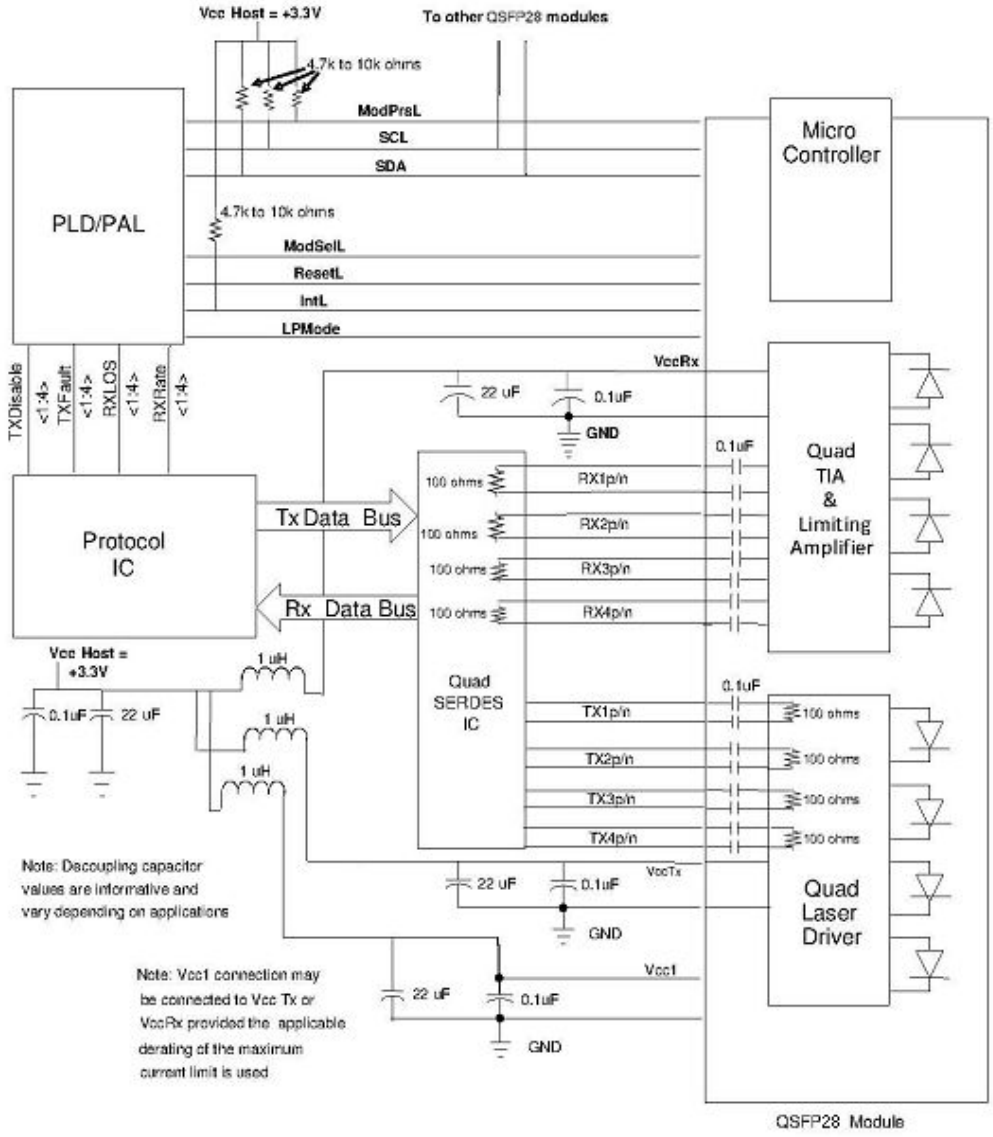
The operating and diagnostics information is monitored and reported by a Digital Diagnostics Transceiver Controller inside the transceiver, which is accessed through the 2-wire serial interface. When

the serial protocol is activated, the serial clock signal (SCL pin) is generated by the host. The positive edge clocks data into the QSFP28 transceiver into those segments of its memory map that are not write-protected. The negative edge clocks data from the QSFP28 transceiver. The serial data signal (SDA pin) is bi-directional for serial data transfer. The host uses SDA in conjunction with SCL to mark the start and end of serial protocol activation. The memories are organized as a series of 8-bit data words that can be addressed individually or sequentially. The 2-wire serial interface provides sequential or random access to the 8 bit parameters, addressed from 00h to the maximum address of the memory.

This clause defines the Memory Map for QSFP28 transceiver used for serial ID, digital monitoring and certain control functions. The interface is mandatory for all QSFP28 devices. The memory map has been changed in order to accommodate 4 optical channels and limit the required memory space. The structure of the memory is shown in Figure 2 -QSFP28 Memory Map. The memory space is arranged into a lower, single page, address space of 128 bytes and multiple upper address space pages. This structure permits timely access to addresses in the lower page, e.g. Interrupt Flags and Monitors. Less time critical entries, e.g. serial ID information and threshold settings, are available with the Page Select function. The structure also provides address expansion by adding additional upper pages as needed. For example, in Figure 2 upper pages 01 and 02 are optional. Upper page 01 allows implementation of Application Select Table, and upper page 02 provides user read/write space. The lower page and upper pages 00 and 03 are always implemented. The interface address used is A0xh and is mainly used for time critical data like interrupt handling in order to enable a “one-time-read” for all data related to an interrupt situation. After an Interrupt, IntL, has been asserted, the host can read out the flag field to determine the effected channel and type of flag.

For more detailed information including memory map definitions, please see the QSFP28 MSA Specification.

VII. Host - Transceiver Interface Block Diagram



VIII. Outline Dimensions