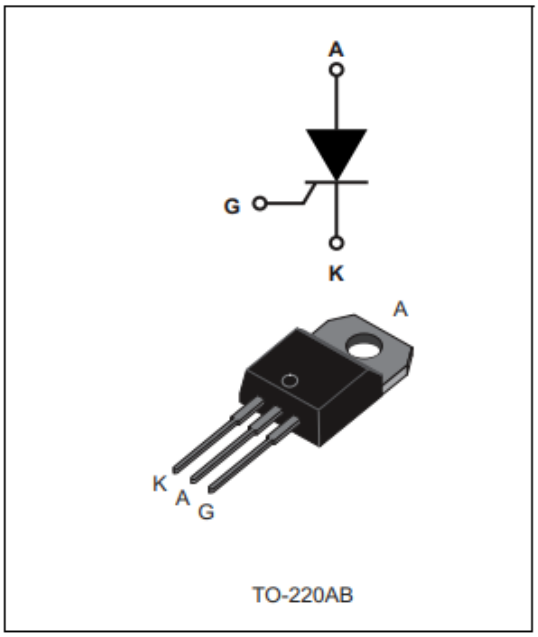
Yangzhou Positioning Tech. Co., Ltd

Thyristor

P/N:YZPST-25TTS12FP

●DESRCRIPTION:

Due to separation diffusion process and mesa technology and Glass passivation, these devices have good performance at dv/dt and reliability. These series of SCR are specifically designed for domestic lighting, heating and motor speed controllers.



●MAIN FEATURES

Symbol	Value	Unit
$I_{T(RMS)}$	25	A
V_{DRM}/V_{RRM}	1200	V
I_{GT}	10-20	mA

●ABSOLUTE MAX I MUM RATINGS

Symbol	PARAMETER			Value	Unit
$I_{T(RMS)}$	RMS on-state current(all conduction angles)	TO-220AB	Tc=90℃	25	A
I_{TSM}	Non repetitive surge peak on-state current (half sine cycle, Tj=25℃)	F=50HZ	t_p=10ms	250	A
I^2t	I^2t Value for fusing	t_p=10ms		312	A^2S
di/dt	Repetitive rate of rise of on-state Current after triggering	F=120HZ,Tj=125℃		100	A/μs
V_{DRM} V_{RRM}	Repetitive Peak Off-state Voltage Repetitive Peak Reverse Voltage	T_j=25℃		1200	V
I_{GM}	Peak gate current, t_p=20us,	T_j=125℃		4	A
$P_{G(AV)}$	Average gate power dissipation	T_j=125℃		1	W
T_{stg}	Storage junction temperature range	-40 to +150			℃
T_j	Operating junction temperature range	-40 to +125			℃

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●ELECTRICAL CHARACTERISTICS

Symbol	Test Condition	Quadrant	Value		Unit
I_{GT}	V_{AK}=12V, R=50Ω, T=25℃	Ⅰ	MAX	25	mA
V_{GT}	V_{AK}=12V, R=50Ω, T=25℃	Ⅰ	MAX	1.2	V
V_{GD}	V_D=V_{DRM} R_L=3.5KΩ Tj=125℃		MIN	0.2	V
I_H	I_T=100mA, I_G=50mA		MAX	50	mA
I_L	I_G=1.2I_{GT}	Ⅰ	MAX	80	mA
dv/dt	V_D=67% V_{DRM} gate open(Tj=125℃)		MIN	1000	V/μs

●STATIC CHARACTERISTICS

Symbol	Parameter	Value		Unit
V_{TM}	I_T=50A, I_G=50mA, T=25℃	MAX	1.50	V
I_{DRM}/I_{RRM}	V_D=V_{DRM} V_R=V_{RRM}, T_j=25℃	MAX	5	μA
H.T.I_{DRM}/I_{RRM}	V_D=V_{DRM} V_R=V_{RRM}, T_j=125℃	MAX	1	mA
$R_{th(j-c)}$	Junction to case(DC), TO-220A	MAX	0.9	℃/W

●ELECTRICAL CHARACTERISTICS (CURVES)

Figure 1. Maximum power dissipation versus average on-state current

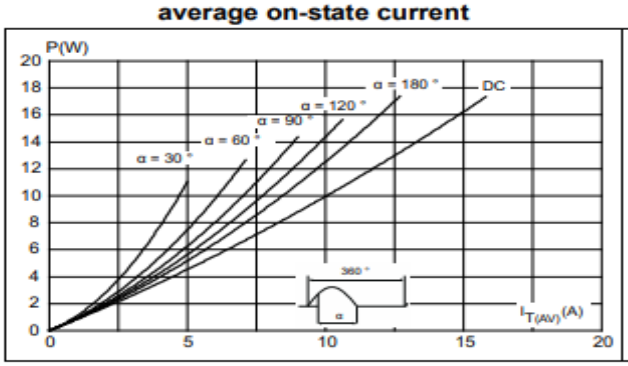

Figure 2. Average and DC on-state current versus case temperature

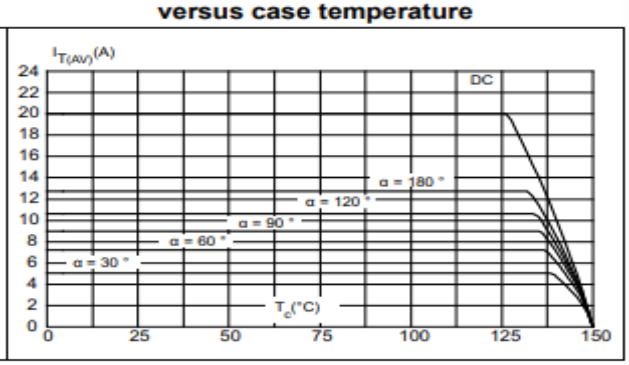

Figure 3. Average and DC on-state current versus ambient temperature

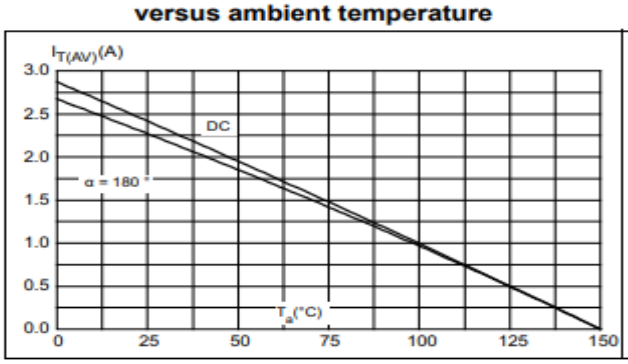

Figure 4. Relative variation of thermal impedance versus pulse duration

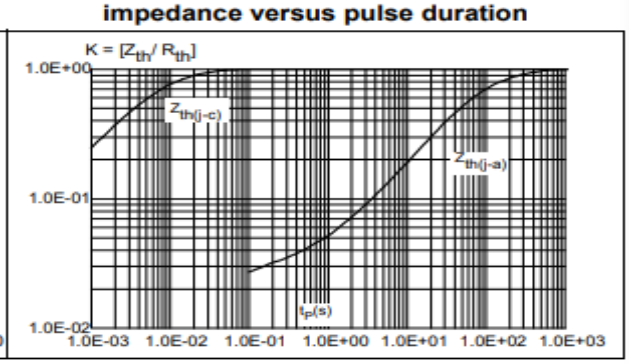

Figure 5. Relative variation of gate triggering current and gate voltage versus junction temperature (typical values)

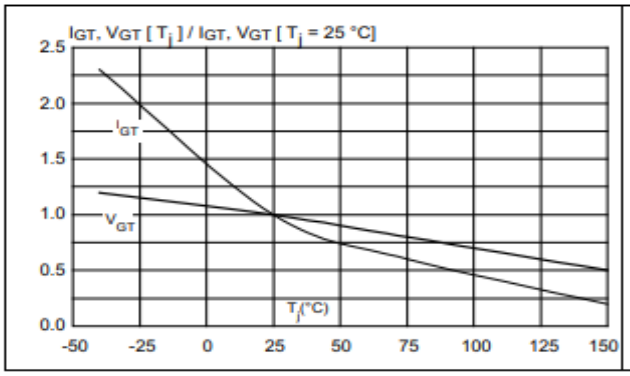

Figure 6. Relative variation of holding current and latching current versus junction temperature (typical values)

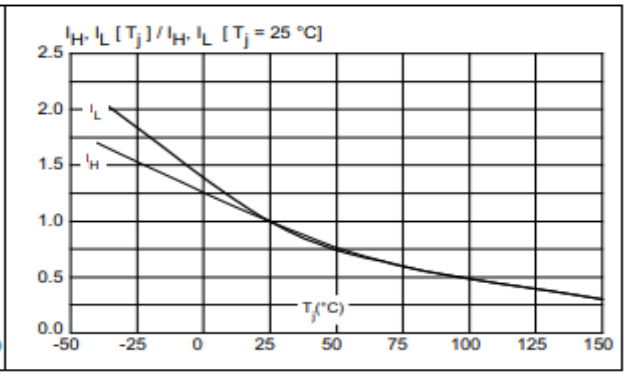

Figure 7. Relative variation of static dV/dt immunity versus junction temperature (typical values)

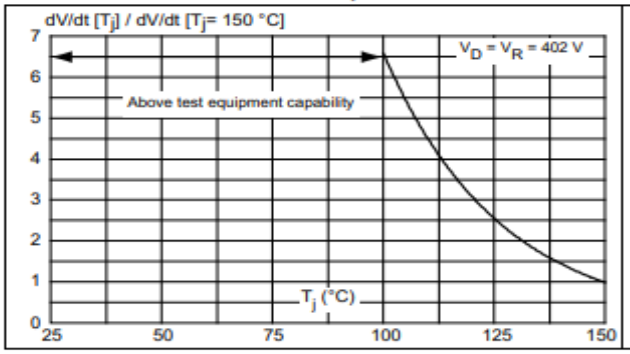

Figure 8. Surge peak on-state current versus number of cycles

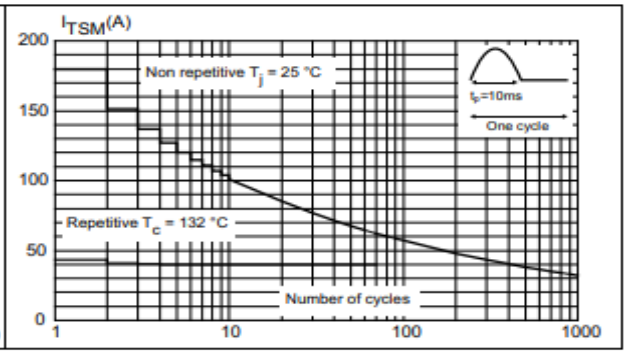

Figure 9. Non-repetitive surge peak on-state current for a sinusoidal pulse (tp < 10 ms)

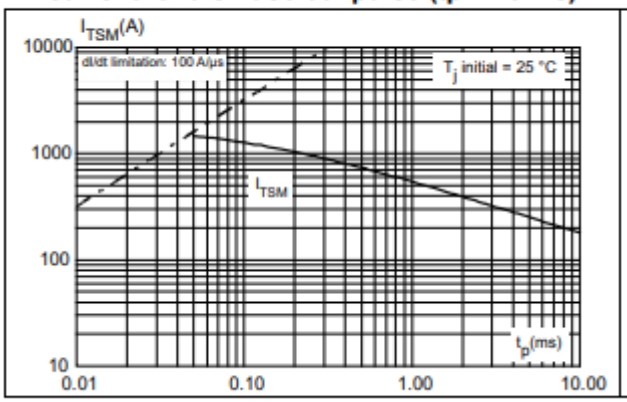

Figure 10. On-state characteristics (maximum values)